Dynamic Response of Jospephson Resistive Logic (DCI) GATE

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ABSTRACT ----- In this paper a thorough investigation of resistive logic gate DCI has been made. The current equations of this gate at each stage have been deduced. The dynamic response of this DCI gate has been obtained by the computer-simulation. Our concept of turn-on delay has been introduced. The effect of overdrive current on turn-on delay for resistive logic gate has been shown. This will provide a better understanding of switching dynamics of the DCI logic gate. Further, we have shown the effect of overdrive current on this logic gate.

1. INTRODUCTION

Two attractive features of SQUID devices for logic applications are isolation and serially connected fan-out. The isolation is provided by the transformer coupling between the SQUID and the input. The isolation is not perfect in the sense that a noise pulse (typically 5 percent) is fed back into the control line when the SQUID switches to the non-zero voltage. The other advantage is the serial fan-out capability by which the control lines of many load devices can be connected in series with a single output line.

The main drawbacks of SQUID devices for logic application are relatively large device area and high sensitivity to stray magnetic fields. In SQUID 80% of the area is occupied by the transformer [1]. Further, the high sensitivity to stray magnetic field requires that the SQUID based logic circuits be well shielded from the stray magnetic fields.

The resistive logic gates such as JAWS (Josephson Auto-Weber System) [2], DCI (Direct Coupled Isolation) [3] and RCJL (Resistor Coupled Josephson Logic) [4] are chosen because the gate logic delay in this case would consist of the turn-on delay, switching delay and propagation delay, but not the crossing delay as in the case of magnetically coupled logic gates. Further, these resistive logic gates do not have a factor of limiting the size very seriously. So, the gate propagation delay can be made sufficiently small. Therefore, the small time constant of the Josephson junction can be directly attained to these gates.

It has been considered by the earlier workers [5] that the turn-on delay of a logic gate is the time taken for the logic gate to obtain 2% of the output current to the load. This consideration seems to be orbitrary.

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Due to this fact, in the present paper we have made a thorough investigation of the resistive logic gates. Our concept of turn-on delay [6] has been introduced which will be able to remove the confusion in critically ascertaining the switching speed of these logic gates. Further, the effect of overdrive current on these resistive logic gates has been studied.

2. DCI (DIRECT COUPLED ISOLATION)

This was proposed by Gheewala et al [3]. Here the Josephson junction is used just a so called "diode" junction - connecting the input signal to logic device to provide isolation.

It consists of two Josephson junctions J1 and J2 as shown in Fig.1. The junctions J1 has a critical current Io and junction capacitance Cj, and the junction J2 has a critical current 2 Io and the junction capacitance 2Cj. The resistances of R1 and R2 are r and r/2 respectively. The DCI gate is biased in the superconducting state by the injection of the input current Iin. The junction J2 plays the role of the current-summing junction in this gate.

When the input signal Iin is directly injected to this DCI gate, it will add to the bias current in junction J2 and substract from the bias in junction J1. The junction J2 is a current-summing junction which switches first to non-zero voltage state. This makes J2 highly resistive, steering most of the signal and the gate current to ground through the resistor R1 (RL >> R1). The gate current Ig is selected to be sufficient to then switch J1 to the non-zero voltage state. With both J1 and J2 in the high-resistance state, the gate current is steered to the RL and signal current to ground via the resistor R1. The high-resistance of J1 prevents gate current from feeding back into the input signal line and thus provides isolation. However, the isolation is not perfect and a small amount of current (typically 3-5 percent) is fed back into the input line.

The above DCI gate can be modified or converted to a JAWS gate (as shown Fig.2). Here two differences are there between DCI and JAWS gates, one is the Ioff current is absent for DCI gate and the other one is that the extra resistor R2 is connected in series with the junction J2.

According to Fig.2 the current equations at each statge of the DCI gate can be written as:

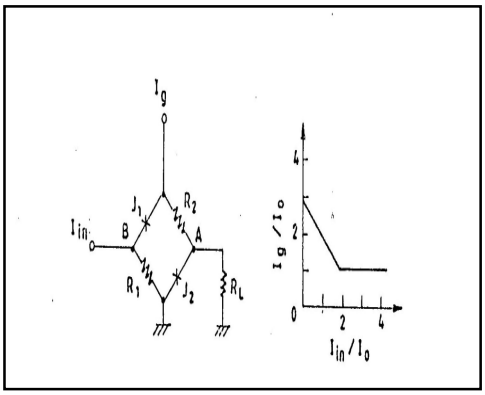

Fig.1 Circuit configuration of the resistive DCI logic gate with threshold characteristics

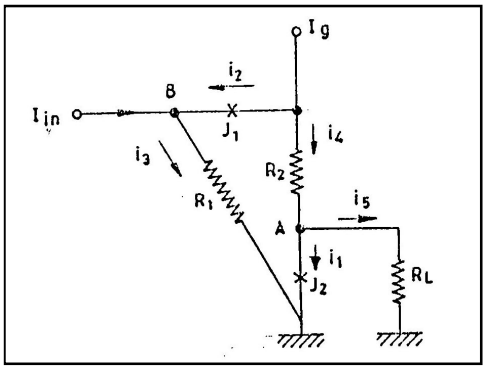

Fig. 2 Circuit configuration of the resistive DCI logic gate with current indication at each stage of the logic gate.

$$i_1 = 2I_o \sin\theta_a + 2C_j \frac{dVa}{dt} \quad \text{---- (1)}$$

$$i_2 = I_o \sin(\theta_a - \theta_b) + C_j \frac{d}{dt}(V_a - V_b) \quad \text{---- (2)}$$

$$i_3 = \frac{V_a}{R_1} \quad \text{---- (3)}$$

$$i_4 = \frac{V_a}{R_2} \quad \text{---- (4)}$$

$$i_5 = \frac{V_a}{r_L} \quad \text{---- (5)}$$

$$V_a = \frac{\phi_o}{2\pi}\frac{d\theta_a}{dt} \; ; \; V_b = \frac{\phi_o}{2\pi}\frac{d\theta_b}{dt} \quad \text{----(6)}$$

$$I_g = i_2 + i_4 \; ; \; i_4 = i_1 + i_5 \quad \text{---- (7)}$$

$$I_{in} + i_2 = i_3 \quad \text{---- (8)}$$

(Note : Here the effect of subgap quasiparticle resistance Rj has been neglected since Ri >> r, rL).

(a) Static case

$$At\ t = 0,\ V_a = V_b = 0 \Longrightarrow$$

$$\frac{d\theta_a}{dt} = \frac{d\theta_b}{dt} \Longrightarrow i_3 = i_4 = 0$$

After using the above conditions in Eqns.(6.3.1) and (6.3.2) we obtain,

$$\frac{I_g}{I_o} = 2\sin\theta_a - \frac{I_{in}}{I_o} \quad \text{---- (I)}$$

Egn.(I) describes the static behaviour of DCI gate. A static curve between 1g/Io and Iin/Io will give the operating margin and gain margins of the DCI gate.

(b) Dynamic case

Eqn. (1) can be written as

$$i_1 = 2I_o \sin\theta_a + 2C_j \frac{d^2\theta_a}{dt^2}\frac{\phi_o}{2\pi}$$

$$or\ \frac{d^2\theta_a}{dt^2} = \frac{\pi}{\phi_o C_j}[i_1 - 2I_o \sin\theta_a] \quad \text{---- (8)}$$

Similarly. Egn.(2) can be written as,

$$\frac{d^2\theta_b}{dt^2} = \frac{2\pi}{\phi_o C_j}[\frac{i_1}{2} - i_2 - 2I_o \sin\theta_a + I_o \sin(\theta_a - \theta_b)] \quad \text{---- (9)}$$

Further, from Eqns. (6) and (7) we get,

$$i_1 = I_g + I_{in} - (i_3 + i_4)$$

$$i_2 = -I_{in} + i_3$$

Substituting the above values il and i2 in Egns.(8) and (9) we obtain,

$$\frac{d^2\theta_a}{dt^2} = \frac{\pi}{\phi_o C_j}[I_g + I_{in} - 2I_o \sin\theta_a - \frac{\phi_o}{2\pi R_1}\frac{d\theta_b}{dt} - \frac{\phi_o}{2\pi r_L}\frac{d\theta_a}{dt}] \quad \text{--- (II)}$$

$$and\ \frac{d^2\theta_b}{dt^2} = \frac{2\pi}{\phi_o C_j}[\frac{I_g}{2} + \frac{3}{2}I_{in} - 2I_o \sin\theta_a + I_o \sin(\theta_a - \theta_b)$$

$$-\frac{3\phi_o}{4\pi R_1}\frac{d\theta_b}{dt} - \frac{\phi_o}{4\pi r_L}\frac{d\theta_a}{dt}\ ] \qquad \text{---(III)}$$

Computer-simulated pulse response of the DCI gate can be obtained by solving the Eqns. (II) and (III) for an input current Iin applied as a step function at t=0 with amplitude 1.5 Ith. To solve these equations the initial conditions for θa (θao) and θb (θbo) are to be known which can be deduced as follows:
At t = 0 from Egns. (6) and (7), we have,

$$I_g = i_1 + i_2 \quad and\ i_2 = 0$$

$$or\ \theta_{ao} = \sin^{-1}\left(\frac{I_g}{2I_o}\right) \qquad \text{--- (a)}$$

$$and\ \theta_{ao} = \theta_{bo}$$

The dynamic response of the DCI gate at each stage (shown in Fig.3) have been obtained from commputer simulation. The DCI logic gate characterstics are similar to JAWS gate, and have advantages over JAWS in the better margin and gains due to the lack of Ioff (offset) current.

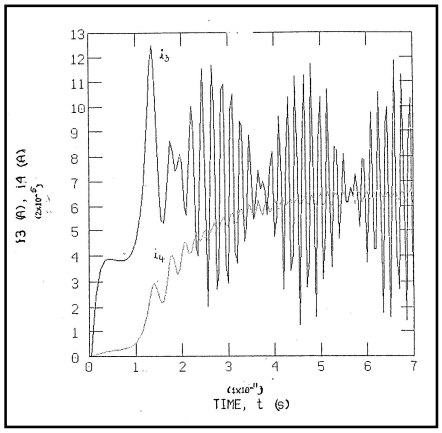

Fig. 3 Simulated switching dynamics of the DCI gate. Circuit parameters used in the simulaton are from Nb/A10x/Nb Josephson technology and are given as Io = 0.087 mA, Cj = 0.37 pF, R1 = R2 = 0.8 Ω, rL = 10 Ω. The swithching waveforms current flowing in the input resistor R and the output current respectively.

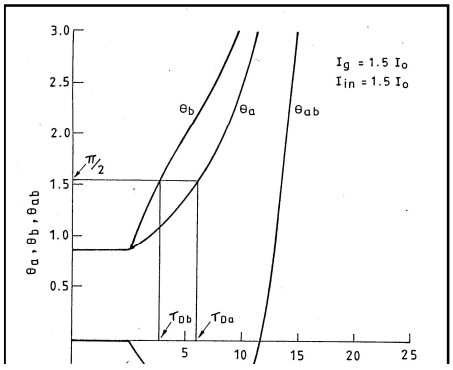

Fig. 4 Simulated phase evolution vs time for a DCI gate. θa and θab are the phase differences of the junctions J1 and J2, respectively. Io = 0.087 mA, Cj = 0.37 pF, R1 = R2 = 0.8 Ω and rL = 10 Ω.

In Fig.4 we have shown the phase variations with time at different stages of the DCI gate (shown in Fig.2). The biasing and overdrive current conditions are as follows: Ig = 1.5 Io and Iin = 1.5 Io.
Using our concept of turn-on delay [6], the turn-on delay at each stage of the DCI has been indicated as shown in the Fig-2. This will give an exact physical understanding of switching dynamics of the DCI logic gate.

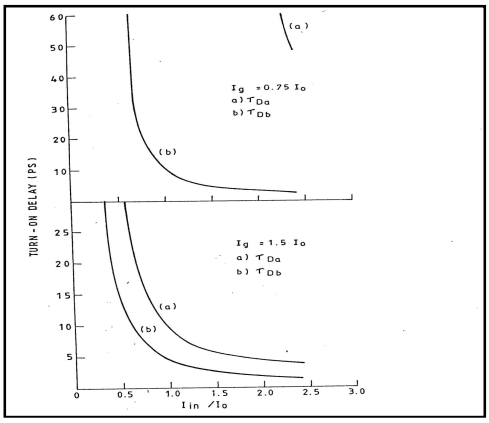

Fig. 5a Turn-on delay of the DCI gate vs input current. TDa and TDb represent the turn-on delay variation with time at point 'a' and 'b' respectively (as shown in Fig.2)

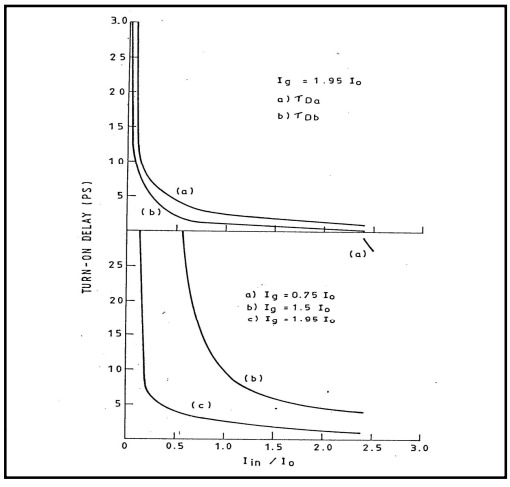

Fig. 5b Turn-on delay of the DCI gate vs input current. TDa and TDb represent the turn-on delay variation with time at point 'a' and 'b' respectively (as shown in Fig.2)

Also we have plotted (in Fig.5a and Fig.5b) the effect of overdrive current on turn-on delay for different biasing conditions Ig = 0.75 I0, 1.5 Io and 1.95 Io. In Fig. 5a the curve (a) indicates the TD variation with overdrive at the point 'A' (as shown in Fig.2) and the curve (b) indicates the TD variation with overdrive at the point 'B'. It can be observed from Fig.5, the turn-on delay decreases as the overdrive increases. Also, the turn-on delay increases with increase of biasing rate. So, by choosing high biasing and overdrive currents, we can minimize the turn-on delay of the DCI logic gate.
Further, for the same overdrive and biasing conditions (Ig = 1.5 Io; Iin = 1.5 Io) the turn-on delay of the DCI gate is smaller than that of JAWS gate. . In a similar manner a thotough investigation of other resistive logic gates, DCI logic gate [7} and RCJL gate[8] have been made which gives better understanding of logic gates before they could be fabricated experimentally.

3. CONCLUSIONS

A thorough investigation of DCI logic gate has been made . The dynamic response of this logic gate is obtained by computer-simulation. The concept of our turn-on delay has been introduced which has helped us in critically ascertaining the switching speed of the logic gate. The effect of turn-on delay on overdrive current has been studied. It is observed that for low fan-outs, the DCI logic gate seems to be a better choice for logic circuit application. It is expected that the concept of turn-on delay will be able to remove confusions which are lying in the earlier investigations.

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